IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Before the Board of Patent Appeals and Interferences

In re Patent Application of Atty Dkt. 550-299
C# M#

SLOBODNIK et al TC/A.U.: 2133

Serial No. 10/025,816 Examiner: J. Tabone, Jr.

Filed: December 26, 2001 Date: November 14, 2005

Title: METHOD AND APPARATUS FOR MEMORY SELF TESTING

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

☐ **Correspondence Address Indication Form Attached.**

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Applicant hereby **appeals** to the Board of Patent Appeals and Interferences from the last decision of the Examiner twice/finally rejecting applicant's claim(s). $500.00 (1401)/$250.00 (2401) $

☒ An appeal **BRIEF** is attached in the pending appeal of the above-identified application $500.00 (1402)/$250.00 (2402) $ 500.00

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☐ A reply brief is attached. **(no fee)**

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By Atty: Stanley C. Spooner, Reg. No. 27,393

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application of
SLOBODNIK et al
Serial No. 10/025,816
Filed: December 26, 2001

Confirmation No.: 4369
Atty. Ref.: 550-299
Group: 2138
Examiner: J. Tabone, Jr.

For: METHOD AND APPARATUS FOR MEMORY SELF TESTING

* *

APPEAL BRIEF

On Appeal From Group Art Unit 2138

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TABLE OF CONTENTS

I. REAL PARTY IN INTEREST 1

II. RELATED APPEALS AND INTERFERENCES 1

III. STATUS OF CLAIMS 2

IV. STATUS OF AMENDMENTS 2

V. SUMMARY OF THE CLAIMED SUBJECT MATTER 2

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL 6

VII. ARGUMENT 6

A. The Examiner has failed to properly construe the language of Appellants' independent claims 1 and 18 8

B. The Lo reference fails to include structures and method steps set out in properly construed independent claims 1 and 18 9

C. The Examiner fails to allege that the claim language missing from the Lo reference is disclosed in either the Gold or Correale references 16

D. The Examiner fails to provide any "reason" or "motivation" for combining any of the Lo, Gold and Correale references 17

VIII. CONCLUSION 19

IX. CLAIMS APPENDIX A1

X. EVIDENCE APPENDIX A12

XI. RELATED PROCEEDINGS APPENDIX A13

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application of

SLOBODNIK et al — Atty. Ref.: 550-299

Serial No. 10/025,816 — Group: 2133

Filed: December 26, 2001 — Examiner: J. Tabone, Jr.

For: METHOD AND APPARATUS FOR MEMORY SELF TESTING

* *

November 12, 2005

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Sir:

I. REAL PARTY IN INTEREST

The real party in interest in the above-identified appeal is ARM Limited by virtue of an assignment of rights from the inventors to ARM Limited recorded April 16, 2002 at Reel 12799, Frame 210.

II. RELATED APPEALS AND INTERFERENCES

There are believed to be no related appeals, interferences or judicial proceedings with respect to the present application and appeal.

III. STATUS OF CLAIMS

Claims 1-34 stand rejected in the outstanding Final Official Action. The Examiner contends that claims 1-9, 13, 16-26, 30 and 33 are anticipated under 35 USC §102 by Lo (U.S. Patent 5,661,732). The Examiner also contends that claims 10-12, 14, 15, 27-29, 31 and 32 are obvious under 35 USC §103 over Lo in view of Gold (US Publication No. 2003/0167428) or Correale (U.S. Patent 6,001,662).

IV. STATUS OF AMENDMENTS

No amendments have been submitted with respect to the Final Rejection. A Pre-Appeal Brief Request for Review was filed concurrent with the noting of this appeal and the Decision mailed October 19, 2005 indicated that this appeal should proceed to the Board of Patent Appeals and Interferences.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

The present invention relates to the field of built-in self-test systems for data processors.

As data processing systems are often fabricated in bulk on silicon wafers which are later cut into individual dies, as memory sizes increase the proportion of the area of an individual die taken up by the memory increases. The higher transistor density (transistors are used to store the memory data) within the memory increases the defect density of those memories. It is desirable to be able

to quickly and efficiently test all transistor circuits in a manufactured memory system, but as can be appreciated, this will necessitate the testing of many millions of circuits.

It is well known to utilize self-test circuits in such memory systems so as to conveniently be able to test and ensure correct fabrication of the memory system. Self-test circuits themselves will take up a certain amount of "circuit area overhead" and, if this area needed by the test circuits can be reduced, then circuit area is available for additional memory.

The Appellants recognized that in some circumstances a programmable self-test controller, which allows different test methodologies to be performed on the chip memory system is desirable. Appellants also found that a programmable self-test controller is advantageous over a conventional self-test controller which merely carries out a single test methodology. However, the programmable self-test controller does slightly increase the size and complexity of the controller in a manner which would generally be regarded as disadvantageous.

Appellants found that in spite of this apparent disadvantage, programmable self-test controllers and their ability to re-use the self-test controller design to cope with different test requirements of different manufacturers or different test requirements that may arise from a single manufacture with different fabrication processes is highly advantageous. Appellants found that a self-test controller can

be driven by a program of self-test instructions which guide the controller to carry out whatever test methodology is desired by a particular user.

In one embodiment of the present invention, a given test methodology (where the conventional dictionary definition of "methodology" is "a body of methods, rules and postulates employed by a discipline: a particular procedure or set of procedures" *Webster's Ninth New Collegiate Dictionary*) is synthesized in the self-test controller and fixed in hardware such that the test methodology can be implemented in response to a self-test instruction. As a result, in accordance with the present invention, a given test methodology can be completely specified by a single self-test instruction.

Various examples of test methodologies according to embodiments of the present invention are provided in Appellants' specification from page 10, line 20 to page 11, line 16. For example, the self-test controller 10 with an included state maching 22 can provide a sequence of test steps comprising a test methodology to the memory array 18. A single self-test instruction can be used to request an increment decrement wordline fast march test (00110) or a bang test (01010) (or other specified test) to be accomplished (see the table on page 21 of Appellants' specification).

For prior art systems such as those disclosed in the Lo patent (U.S. Patent 5,661,732), to implement a word line fast march test requires microcode array 10 to be loaded with about six 9-bit microcode words (i.e., cell rows). The first cell

row would have a 3-bit data field which would specify constant data for the write of array. The second cell row would have the same 3-bit field for read data. The third cell row would indicate opposite data for the write. The third cell row would also indicate a jump back to the second cell row to loop until address expires and so on. After executing this test, the Lo microcode array would have to be reloaded to perform a different test. There is no capability or provision in Lo for the self-test controller to be responsive to a single self-test instruction or to implement different self-test methodologies.

However, with the present invention, a single self-test instruction can be loaded which causes a memory test methodology (sequence of steps) to be applied which methodology can include a sequence of memory storage locations to be accessed. This system gives the advantage of flexibility in testing which can be applied without placing an undue burden upon users by requiring them to have a highly detailed knowledge of the inner workings of the self-test controller.

The present invention claimed in apparatus claim 1 and method claim 18 is characterized by an apparatus for testing a memory system in which the memory has a plurality of storage locations, and a self-test controller for controlling self-test of the memory where the self-test controller is responsive to a "**self-test instruction specifying a test methodology to be applied**" (emphasis added) where memory address changes are selected in dependence upon the self-test instructions. In addition, claims 1 and 18 require that the self-test controller may

be "**configured by said self-test instruction to implement different memory test methodologies.**" (emphasis added). As will be seen, neither of the above aspects of claims 1 and 18 are shown or obvious in view of the cited Lo patent.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-9, 13, 16, 17, 18-26, 30 and 33 stand rejected under 35 USC §102 as being anticipated by Lo (U.S. Patent 5,661,732), with the Examiner contending that Lo teaches every element and method step set out in independent claims 1 and 18, including a self-test controller which is "responsive to a self-test instruction" and which is "configured by said self-test instruction to implement different memory test methodologies."

Claims 10, 11, 14, 27, 28 and 31 stand rejected under 35 USC §103 as unpatentable over Lo in view of Gold (US Publication 2003/0167428) and Claims 12, 15, 29 and 32 stand rejected under 35 USC §103 as unpatentable over Lo in view of Correale (U.S. Patent 6,001,662).

VII. ARGUMENT

Appellants' arguments include the fact that the burden is on the Examiner to first and foremost properly construe the language of the claims to determine what structure and/or method steps are covered by that claim. After proper construction of the claim language, the burden is also on the Examiner to

demonstrate where a single reference (in the case of anticipation) or a plurality of references (in the case of an obviousness rejection) teaches each of the structures and/or method steps recited in independent claims 1 and 18.

The Court of Appeals for the Federal Circuit has noted in the case of *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick*, 221 USPQ 481, 485 (Fed. Cir. 1984) that "[a]nticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim."

Furthermore, the Court of Appeals for the Federal Circuit has stated in the case of *In re Rouffet*, 47 USPQ2d 1453, 1458 (Fed. Cir. 1998)

"to prevent the use of hindsight based on the invention to defeat patentability of the invention, this court **requires** the examiner to show a **motivation** to combine the references that create the case of obviousness. In other words, the Examiner **must show reasons** that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed." (emphasis added).

A. The Examiner has failed to properly construe the language of Appellants' independent claims 1 and 18

Prior to conducting any analysis on the merits, it is necessary that the Examiner properly construe the language of Appellants' claims. All claim terms must be understood and correctly interpreted in order to appreciate the correct scope of the claim.

Both of appellant's independent apparatus claim 1 and method claim 18 require "a self-test instruction specifying a test methodology." Each of these claims indicate that the self-test controller is responsive to such "self-test instruction specifying a test methodology."

The term "methodology" is well known to those of ordinary skill in the art, and the conventional definition in *Webster's Ninth New Collegiate Dictionary* is "a body of methods, rules, and postulates employed by a discipline: a particular procedure or set of procedures." This definition is consistent with the use of the term "methodology" in the specification to mean a sequence of steps and not a single step.

Thus, the conventional definition and the use of the term in the specification makes it clear that "methodology" cannot be a single step, single rule or a single postulate. Rather, a methodology and the use of that term in the appellant's claims requires a sequence of steps, rules and/or postulates.

The Examiner apparently ignores the conventional definition of "methodology" and the use of this tem consistent with the conventional definition in his application of the Lo reference. As will be seen, he takes a reference that discloses a single step and erroneously construes this to suggest a sequence of a plurality of steps, rules and/or postulates, i.e., a "methodology."

Thus, the Examiner is bound by the definition of the word "methodology" and to anticipate or render obvious the subject matter of Appellants' claims, he must find that the prior art discloses a "self-test instruction specifying a test methodology" and a self-test controller that may be configured "by said self-test instruction to implement different memory test methodologies."

The Examiner's failure to properly construe the "methodology" term in Appellants' independent claims 1 and 18 is fatal to his rejection of these claims and any further rejection of claims 1 and 18 and any claims dependent thereon is respectfully traversed.

B. The Lo reference fails to include structures and method steps set out in properly construed independent claims 1 and 18

As noted above, "[a]nticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." *Lindemann*. Thus, the burden is on the Examiner, in order to support his anticipation rejection of claims 1 and 18, to show where in the single

cited reference of Lo, each and every element of Appellants' claims is clearly and unequivocally disclosed therein.

1. The Lo reference fails to teach or suggest a self-test controller which is "responsive to a self-test instruction specifying a test methodology"

The Examiner states on page 4, section 4 of the Final Rejection that "Lo discloses that the ABIST engine 12 (self-test controller) receives a 9 bit word 13 from a Microcode Array 10 which stores a set of test program codes scanned-in prior to ABIST test (self-test controller configured by self-test instruction)." In effect, the Examiner is contending that one of the Lo 9-bit microcode words specifies "a test methodology." However, the Examiner's conclusion is incorrect.

Each of the cited 9-bit microcode words teaches only a single step. While the Lo controller stores up to eight different 9-bit microcode words, none of them contain anything more than the teaching of a single step. All of the eight microcode words are needed to implement a single test methodology or sequence of steps.

Appellants have repeatedly challenged the Examiner to demonstrate how or where any microcode word in the Lo patent teaches or defines a test methodology and the Examiner has been unable to comply with Appellants' request. In fact the discussion in Lo teaches the direct opposite, i.e., that a sequence of words is necessary to define the methodology.

For example, if the Examiner reviews the entire Lo document, he will note that the section entitled "Micro-Programming Examples" (from column 12 to column 16) which details how different test methodologies must be implemented in the Lo system. Lo discloses (as discussed at column 4, lines 33-37 with reference to Figure 1) that each of the 9-bit microcode words comprise a 3-bit pointer field 13, a 1-bit address increment field 15, a 3-bit data control field 16, a 1-bit write control field and a 1-bit end of address space control field 18. There is no indication that a single 9-bit word can specify a sequent of test steps, i.e., a methodology.

The Examiner contends in section 3 of the Official Action that the 3-bit data control field 16 disclosed in column 10 of Lo specifies a "test methodology" to be applied, i.e., walking, marching, checker-board, column-stripe, etc. However, this is not the case, because to implement a test methodology, a plurality of 9-bit microcode words are required. Lo, between columns 12 and 16, specifies a number of different microcode programming examples corresponding to different tests. For example, column 13, lines 7-19 (Example 4) of Lo lists eight 9-bit microcode words that are required to implement a checkerboard test. Similarly, column 15, lines 26-50 of Lo specifies two different walking tests, each comprising eight 9-bit microcode words. Considering the checkerboard test, it is not sufficient to simply specify the data pattern control field 111 in a single 9-bit microcode word in order to implement this test as the Examiner asserts on the

basis of the Lo Table 7. Rather, the total of all eight 9-bit microcode words must be specified in order to teach the particular test.

Thus, the Lo reference fails to teach structure positively recited in independent claims 1 and 18, i.e., a self-test controller which is "responsive to a self-test instruction specifying a test methodology" meaning a series of methods, rules or procedures. Again, should the Examiner believe that Lo teaches a self-test controller which is responsive to a single self-test instruction which specifies a test methodology comprising a plurality of steps, he is respectfully requested to identify any such teaching in the Lo reference.

2. The Lo reference fails to teach or suggest a self-test controller which may be "configured by said self-test instruction to implement different memory test methodologies"

In addition to the requirement that the self-test controller be responsive to a self-test instruction specifying a test methodology, independent claims 1 and 18 also require that the self-test controller may be configured "by said self-test instruction to implement different memory test methodologies."

As noted above, the Examiner has either misconstrued the definition of the term "methodology" or misunderstands the teaching of the Lo patent in that regard. There is no indication that the Lo reference envisions a self-test controller which in any way, shape or form could be configured by a self-test instruction "to implement different memory test methodologies."

Examining Table 7 in the Lo reference at column 10, there are eight microcode words which set a specific test sequence, with the first item having a value of 000 and a meaning of "shift and rotate." As clearly disclosed in Lo, no single value will cause a particular test methodology to operate but rather describe a single step in a methodology. Thus, a knowledge of all of the individual steps are going to be needed by the engineer in devising a proper test methodology, i.e., all eight values set out in Table 7 are necessary to define a single test methodology. Thus, Table 7 in the Lo patent clearly indicates that eight separate 9-bit microcode words are needed in order to define a single methodology, and thus additional microcode words would be necessary to define another methodology. There is simply no suggestion that a single self-test instruction could implement different memory test methodologies as required by Appellants' claims.

By way of contrast, in accordance with the present invention, a given test methodology can be completely specified by a single self-test instruction. Examples of test methodologies according to various embodiments of the invention are provided between page 10, line 20 and page 11 line 16 of the present application.

As a result, it is clear that the Array Built-In Self-Test (ABIST) system of Lo is much less flexible than the self-test controller in accordance with the present invention. While embodiments of the present invention use a single self-test

instruction to perform a "bang" test (see the description on page 11, lines 11 and 12), the microcode array of the Lo patent holds only eight 9-bit microcode words, and thus the Lo system does not even have the capability to perform a "bang" test.

As noted above, in order to implement a test methodology using the Lo patent teaching, the user must program the sequence of steps into the microcode array, requiring a detailed knowledge of such programming. In accordance with the present invention where a self-test instruction specifies a memory test methodology to be applied (including a sequence of memory storage locations to be accessed), it provides the advantage of flexibility of testing which can be applied without placing an undue burden upon users in requiring them to have a highly detailed knowledge of the inner workings of the self-test controller. This renders the self-test controller a more desirable commodity that can be used and re-used by different engineers in different design implementations without significant difficulty. This is clearly a significant benefit over and above the Lo reference.

As before, the Examiner has been requested to point out where or what in the Lo reference he believes evidences a self-test controller which may be "configured by said self-test instruction to implement different memory test methodologies" and no corresponding structure or method step has been identified. In the Examiner's Answer, it is respectfully requested that he specifically identify

any portion of the Lo reference which he believes comprises the claimed self-test controller.

3. There is no basis for a rejection under 35 USC §102

In view of the fact that independent claims 1 and 18 (and the remaining claims dependent thereon) require both (1) a self-test controller which is "responsive" to a self-test instruction specifying a test methodology and (2) a self-test controller which may be configured "by said self-test instruction to implement different memory test methodologies," the burden to establish a proper basis for a rejection under §102 requires that the Examiner clearly demonstrate such structures to be present in the Lo reference.

As noted above, the Examiner has failed to identify any structure in the Lo reference which is either "responsive" to a self-test instruction or which is "configured" by a self-test instruction to implement different memory test methodologies.

In view of such failure, there is simply no support for a rejection of independent claims 1 and 18 and claims dependent thereon as being anticipated under 35 USC §102 in view of the Lo reference.

C. The Examiner fails to allege that the claim language missing from the Lo reference is disclosed in either the Gold or Correale references

Claims 10, 11, 14, 27, 28 and 31 stand rejected as being obvious over the Lo/Gold combination of references and claims 12, 15, 29 and 32 stand rejected as obvious over the Lo/Correale combination of references. Inasmuch as these claims all depend from either claim 1 or claim 18, the above comments relating to the Lo reference are herein incorporated by reference.

The Court of Appeals for the Federal Circuit has consistently held that "the PTO has the burden under §103 to establish a *prima facie* case of obviousness." *In re Fine*, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). The Court went on to state that the PTO "can satisfy this burden only by showing some objective teaching in the prior art . . . ." As noted above, at least two structures/method steps/interrelationships set out in claims 1 and 18 are not present in the Lo reference. Accordingly, in order to support a rejection under 35 USC §103, the Examiner has the burden of showing where those interrelationships are in either the Gold or Correale references.

The Examiner has failed to allege, let alone point out where or how, either the Gold reference or the Correale reference supplies the missing claimed "self-test controller" i.e., one which is "responsive" to a self-test instruction specifying a test methodology or one which may be configured "by said self-test instruction to implement different memory test methodologies." Because the Examiner does not

allege either Gold or Correale to teach or suggest such a self-test controller, these references can be taken as admitted as failing to supply the identified structures and structural interrelationships which are missing from the Lo reference. Again, should the Examiner at this late date contend that the Gold or Correale references do contain such a teaching, he is specifically requested to point out the column and line number of such teachings.

As a result of the above, even if the Lo reference is combined with the Gold reference or the Correale reference, or all three are combined together (which combination is not offered in the Final Rejection), there is simply no teaching of Applicants' claimed "self-test controller." As a result, the Examiner does not have support for a *prima facie* case of obviousness under 35 USC §103 and has clearly failed to meet the required burden.

D. The Examiner fails to provide any "reason" or "motivation" for combining any of the Lo, Gold and Correale references

As noted in the *In re Rouffet* case, in order to prevent the use of hindsight based on applicant's own invention, the Court of Appeals for the Federal Circuit **requires** the Examiner to show a "motivation" to combine references. Specifically, the Examiner must show "reasons" that those skilled in the art confronted with the same problems as the inventor and no knowledge of the invention would select the elements from the prior art in the manner claimed.

With respect to the combination of references and the rejection of claims 10, 11, 14, 27, 28 and 31 over the Low/Gold combination and claims 12, 15, 29 and 32 over the Lo/Correale combination, because none of the references teach Appellants' claimed "self-test controller" (1) which is "responsive" to a self-test instruction specifying a test methodology or (2) which may be "configured by said self-test instruction" to implement different memory test methodologies, the combination of the references does not support the rejection.

The Examiner, in attempting to generate some sort of "motivation," assumes that it would be obvious to make the combination because Appellants' invention has a beneficial result. For example, the Examiner's language on page 9 of the Official Action under claims 11 and 28 state "the artisan would have been motivated to do so because it would enable Lo's ABIST engine 12 (self-test controller) to access the logical addresses of the memory array elements 9." However, the fact that the Appellant's invention provides a valuable benefit is not a motivation to combine elements which do not exist in the prior art. This is precisely the *In re Rouffet* prohibition on using the Appellants' own invention to support an obviousness rejection.

As a result, the Examiner has simply failed to provide any motivation meeting the standards of the Court of Appeals for the Federal Circuit to justify combining elements from the Lo, Gold and Correale references, even if they contained a disclosure of Appellants' claimed "self-test controller."

The Examiner has failed to provide a *prima facie* case of obviousness with respect to claims 10, 11, 14, 27, 28 and 31 over the Lo/Gold combination and claims 12 15, 29 and 32 over the Lo/Correale combination of references.

VIII. CONCLUSION

As noted above, the Examiner fails to point out how or where he believes either prior art reference teaches the subject matter recited in Appellants' independent claims 1 and 18, i.e., a self-test controller which is "responsive to a self-test instruction specifying a test methodology" or that such a self-test controller can be "configured by said self-test instruction to implement different memory test methodologies." If either one of these structures/method steps or structural/method interrelationships is missing from the Lo reference, then the anticipation rejection fails. If either one of these is missing from all three cited references (Lo/Gold/Correale), then the obviousness rejection under 35 USC §103 also must fail. The Examiner has also failed to meet his burden of establishing where such teaching is in any reference and has also failed to establish where there is any "reason" or "motivation" for combining references.

Thus, and in view of the above, the rejection of claims 1-34 under 35 USC §102 or §103 is clearly in error and reversal thereof by this Honorable Board is respectfully requested.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: _____

Stanley C. Spooner
Reg. No. 27,393

SCS:kmm
Enclosure

IX. CLAIMS APPENDIX

1. Apparatus for processing data, said apparatus comprising:

at least one memory having a plurality of memory storage locations associated with respective memory addresses; and

a self-test controller operable to control self-test of said at least one memory; wherein

said self-test controller is responsive to a self-test instruction specifying a test methodology to be applied to perform at least one memory access to each memory location within a sequence of memory storage locations, memory address changes between successive memory locations accessed within said sequence of memory storage locations being selected in dependence upon said self-test instruction such that said self-test controller may be configured by said self-test instruction to implement different memory test methodologies.

2. Apparatus as claimed in claim 1, wherein said self-test controller is operable to execute a plurality of self-test instructions to perform a sequence of memory tests,

said self-test instructions being programmable to allow different sequences of memory tests to be specified by different users.

3. Apparatus as claimed in claim 2, wherein said sequence of memory tests may be changed to match different memories.

4. Apparatus as claimed in claim 2, wherein said sequence of memory tests may be changed to match different fabrication characteristics and test needs.

5. Apparatus as claimed in claim 1, wherein said memory addresses are physical row and column addresses within said at least one memory.

6. Apparatus as claimed in claim 1, wherein said self-test instruction specifies data to be written to said memory as part of said at least one memory access.

7. Apparatus as claimed in claim 1, wherein said memory address changes between successive memory locations as selected in dependence upon said self-test instruction and said self-test controller allow one or more of the following memory test operations to be performed:

(i) write specified data to all memory locations within a range of memory addresses;

(ii) read data from all memory locations within a range of memory addresses; (iii) write specified data to memory locations having a checkerboard pattern of

memory addresses;

(iv) read data from memory locations having a checkerboard pattern of memory addresses;

(v) conduct a march C memory test;

(vi) read data from and write specified data to a sequence of memory locations within a memory arranged in rows and columns of memory locations such that memory locations within a row of memory locations are accessed in turn before a next row of memory locations is selected for access;

(vii) read data from and write specified data to a sequence of memory locations within a memory arranged in rows and columns of memory locations such that memory locations within a column of memory locations are accessed in turn before a next column of memory locations is selected for access;

(viii) read data from, write specified data to and read data from a sequence of memory locations within a memory arranged in rows and columns of memory locations such that memory locations within a row of memory locations are accessed in turn before a next row of memory locations is selected for access;

(ix) read data from, write specified data to and read data from a sequence of memory locations within a memory arranged in rows and columns of memory

locations such that memory locations within a column of memory locations are accessed in turn before a next column of memory locations is selected for access;

(x) for a sequence of memory locations, repeatedly write a value to one or more bitlines within said memory and then read a complementary value stored within a memory location sharing said one or more bitlines;

(xi) for a sequence of memory locations, repeatedly read a value from a memory location while interjecting opposing data writes;

(xii) a predetermined combination of memory test operations as defined in (i) to (xi) for go/nogo testing where manufacture's test methods do not have specific requirements; and

(xiii) creating false read data at specific points in order to validate fail detection.

8. Apparatus as claimed in claim 1, further comprising a processor core, wherein said processor core, said at least one memory and said self-test controller are formed together on an integrated circuit.

9. Apparatus as claimed in claim 1, wherein said at least one memory is a synthesized memory or a custom memory.

10. Apparatus as claimed in claim 1, wherein an interface circuit is disposed between said self-test controller and said at least one memory, said interface circuit serving to adjust values and timings of signals passed between said self-test controller and said at least one memory to accommodate differing value and timing properties of said at least one memory.

11. Apparatus as claimed in claim 10, wherein said interface circuit maps a memory address value generated by said self-test controller to a logical address value to be input to said at least one memory.

12. Apparatus as claimed in claim 1, comprising a plurality of memories and said self-test instruction specifies to which of said plurality of memories said self-test instruction is to be applied.

13. Apparatus as claimed in claim 1, wherein said self-test instruction specifies how a detected memory error is to be reported by said self-test controller.

14. Apparatus as claimed in claim 10, wherein said interface circuit includes a result data register in which result data from testing said at least one memory may be captured and said self-test controller is responsive to a self-test instruction to read result data from said result data register.

15. Apparatus as claimed in claim 1, wherein said self-test instruction specifies a size of said at least one memory to be tested.

16. Apparatus as claimed in claim 1, wherein said self-test instruction is serially loaded into said self-test controller.

17. Apparatus as claimed in claim 1, wherein said at least one memory and said self-test controller are formed together on an integrated circuit having a plurality of external signal pins, said self-test controller having one or more external signal pins through which one or more self-test instructions may be applied to said self-test controller.

18. A method of testing a memory having a plurality of memory storage locations associated with respective memory addresses, said method comprising the steps of:

passing a self-test instruction to a self-test controller coupled to said memory, said self-test instruction specifying a test methodology to be applied; and

in response to said self-test instruction, performing at least one memory access to each memory location within a sequence of memory storage locations, memory address changes between successive memory locations accessed within

said sequence of memory storage locations being selected in dependence upon said self-test instruction such that said self-test controller may be configured by said self-test instruction to implement different memory test methodologies.

19. A method as claimed in claim 18, comprising executing a plurality of self-test instructions with said self-test controller to perform a sequence of memory tests, said self-test instructions being programmable to allow different sequences of memory tests to be specified by different users.

20. A method as claimed in claim 19, wherein said sequence of memory tests may be changed to match different memories.

21. A method as claimed in claim 19, wherein said sequence of memory tests may be changed to match different fabrication characteristics and test needs.

22. A method as claimed in claim 18, wherein said memory addresses are physical row and column addresses within said memory.

23. A method as claimed in claim 18, wherein said self-test instruction specifies data to be written to said memory as part of said at least one memory access.

24. A method as claimed in claim 18, wherein said memory address changes between successive memory locations as selected in dependence upon said self-test instruction and said self-test controller allow one or more of the following memory test operations to be performed:

(i) write specified data to all memory locations within a range of memory addresses;

(ii) read data from all memory locations within a range of memory addresses; (iii) write specified data to memory locations having a checkerboard pattern of memory addresses;

(iv) read data from memory locations having a checkerboard pattern of memory addresses;

(v) conduct a march C memory test;

(vi) read data from and write specified data to a sequence of memory locations within a memory arranged in rows and columns of memory locations such that memory locations within a row of memory locations are accessed in turn before a next row of memory locations is selected for access;

(vii) read data from and write specified data to a sequence of memory locations within a memory arranged in rows and columns of memory locations such that memory locations within a column of memory locations are accessed in turn before a next column of memory locations is selected for access;

(viii) read data from, write specified data to and read data from a sequence of memory locations within a memory arranged in rows and columns of memory locations such that memory locations within a row of memory locations are accessed in turn before a next row of memory locations is selected for access;

(ix) read data from, write specified data to and read data from a sequence of memory locations within a memory arranged in rows and columns of memory locations such that memory locations within a column of memory locations are accessed in turn before a next column of memory locations is selected for access;

(x) for a sequence of memory locations, repeatedly write a value to one or more bitlines within said memory and then read a complementary value stored within a memory location sharing said one or more bitlines;

(xi) for a sequence of memory locations, repeatedly read a value from a memory location while interjecting opposing data writes;

(xii) a predetermined combination of memory test operations as defined in (i) to (xi) for go/nogo testing where manufacture's test methods do not have specific requirements; and

(xiii) creating false read data at specific points in order to validate fail detection.

25. A method as claimed in claim 18, wherein said memory and said self-test controller formed together with a processor core on an integrated circuit.

26. A method as claimed in claim 18, wherein said memory is a synthesized memory or a custom memory.

27. A method as claimed in claim 18, wherein values and timings of signals passed between said self-test controller and said memory are adjusted by an interface circuit disposed between said self-test controller and said at least one memory in order to accommodate differing value and timing properties of said at least one memory.

28. A method as claimed in claim 27, wherein said interface circuit maps a memory address value generated by said self-test controller to a logical address value to be input to said memory.

29. A method as claimed in claim 18, wherein said self-test instruction specifies to which of a plurality of memories said self-test instruction applies.

30. A method as claimed in claim 18, wherein said self-test instruction specifies how a detected memory error is to be reported by

said self-test controller.

31. A method as claimed in claim 27, wherein said interface circuit includes a result data register in which result data from testing said memory may be captured and said self-test controller is responsive to a self-test instruction to read result data from said result data register.

32. A method as claimed in claim 18, wherein said self-test instruction specifies a size of said memory to be tested.

33. A method as claimed in claim 18, wherein said self-test instruction is serially loaded into said self-test controller.

34. A method as claimed in claim 18, wherein said memory and said self-test controller are formed together on an integrated circuit having a plurality of external signal pins, said self-test controller having one or more external signal pins through which one or more self-test instructions may be applied to said self-test controller.

X. EVIDENCE APPENDIX

None.

XI. RELATED PROCEEDINGS APPENDIX

None.